

CLAIMS

What is claimed is:

1. An analog front-end having built-in equalization, the analog front-end comprises:

control module operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front end; and

tunable gain stage operably coupled to amplify and equalize the high-speed serial data based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed serial data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

2. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

a first stage operably coupled to amplify and equalize, to a first level, the high-speed serial data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

3. The analog front-end of claim 2, wherein the second stage further comprises:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

4. The analog front-end of claim 1, wherein the frequency dependent load further comprises at least one high pass filter.

5. The analog front-end of claim 4, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter.

6. The analog front-end of claim 5, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

7. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance

value of the adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed serial data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

8. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;

a second transistor having a gate, a drain, and a source;

a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed serial data, and the drain of the first input transistor is operably

coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed serial data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

9. An analog front-end having built-in equalization, the analog front-end comprises:

a frequency dependent load; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives high-speed serial data and, in conjunction with the frequency dependent load, amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

10. The analog front-end of claim 9, wherein the frequency dependent load further comprises at least one high pass filter.

11. The analog front-end of claim 10, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor, wherein parasitic capacitance of the transistor and the resistor establish a corner frequency for the each of the at least one high pass filter.

12. The analog front-end of claim 11, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the resistor establish the corner frequency for the each of the at least one high pass filter.

13. The analog front-end of claim 9 further comprises:
the frequency dependent load including:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed serial data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

14. The analog front-end of claim 9 further comprises:
the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first resistor operably coupled to the gate and the drain of the first transistor;

a second transistor having a gate, a drain, and a source;

a second resistor operably coupled to the gate and the drain of the second transistor;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed serial data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed serial data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

15. The analog front-end of claim 9 further comprises:
the frequency dependent load including:

a first frequency dependent load; and
a second frequency dependent load;

the amplifier input section including:

a first amplifier input section operably coupled to the first frequency dependent load, wherein the first amplifier input section receives the high-speed serial data and, in conjunction with the first frequency dependent load, amplifies and equalizes the high-speed serial data to produce an intermediate amplified and equalized serial data; and

a second amplifier input section operably coupled to the second frequency dependent load, wherein the second amplifier input section receives the intermediate amplified and equalized high-speed serial data and, in conjunction with the second frequency dependent load,

amplifies and equalizes the high-speed serial data to produce the amplified and equalized serial data.

16. A high-speed data receiver comprises:

an analog front-end operably coupled to amplify and equalize high-speed data to produce amplified and equalized high-speed data; and

clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data, wherein the analog front-end includes:

control module operably coupled to provide a frequency response setting based on a channel response of a channel providing the high-speed data to the analog front end; and

tunable gain stage operably coupled to amplify and equalize the high-speed data based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed data to produce an amplified and equalized serial data.

17. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

a first stage operably coupled to amplify and equalize, to a first level, the high-speed data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

18. The high-speed data receiver of claim 17, wherein the second stage further comprises:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

19. The high-speed data receiver of claim 16, wherein the frequency dependent load further comprises at least one high pass filter.

20. The high-speed data receiver of claim 19, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter.

21. The high-speed data receiver of claim 20, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

22. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

23. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;

a second transistor having a gate, a drain, and a source;

a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

24. A high-speed data receiver comprises:

an analog front-end operably coupled to amplify and equalize high-speed data to produce amplified and equalized high-speed data; and

clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data, wherein the analog front-end includes:

a frequency dependent load; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives high-speed data and, in conjunction with the frequency dependent load, amplifies and equalizes the high-speed data to produce an amplified and equalized serial data.

25. The high-speed data receiver of claim 24, wherein the frequency dependent load further comprises at least one high pass filter.

26. The high-speed data receiver of claim 25, wherein each of the at least one high pass filter further comprises:
a transistor having a gate, a drain, and a source;
a resistor operably coupled to the gate and the drain of the transistor, wherein parasitic capacitance of the transistor and the resistor establish a corner frequency for the each of the at least one high pass filter.

27. The high-speed data receiver of claim 26, wherein the each of the at least one high pass filter further comprises:
a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the resistor establish the corner frequency for the each of the at least one high pass filter.

28. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

29. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:

the frequency dependent load including:

- a first transistor having a gate, a drain, and a source;

- a first resistor operably coupled to the gate and the drain of the first transistor;

- a second transistor having a gate, a drain, and a source;

- a second resistor operably coupled to the gate and the drain of the second transistor;

the amplifier input section including:

- a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

- a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

- current source operably coupled to the sources of the first and second input transistors and to a voltage return.

30. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:

the frequency dependent load including:

a first frequency dependent load; and

a second frequency dependent load;

the amplifier input section including:

a first amplifier input section operably coupled to the first frequency dependent load, wherein the first amplifier input section receives the high-speed data and, in conjunction with the first frequency dependent load, amplifies and equalizes the high-speed data to produce an intermediate amplified and equalized serial data; and

a second amplifier input section operably coupled to the second frequency dependent load, wherein the second amplifier input section receives the intermediate amplified and equalized high-speed data and, in conjunction with the second frequency dependent load, amplifies and equalizes the high-speed data to produce the amplified and equalized serial data.